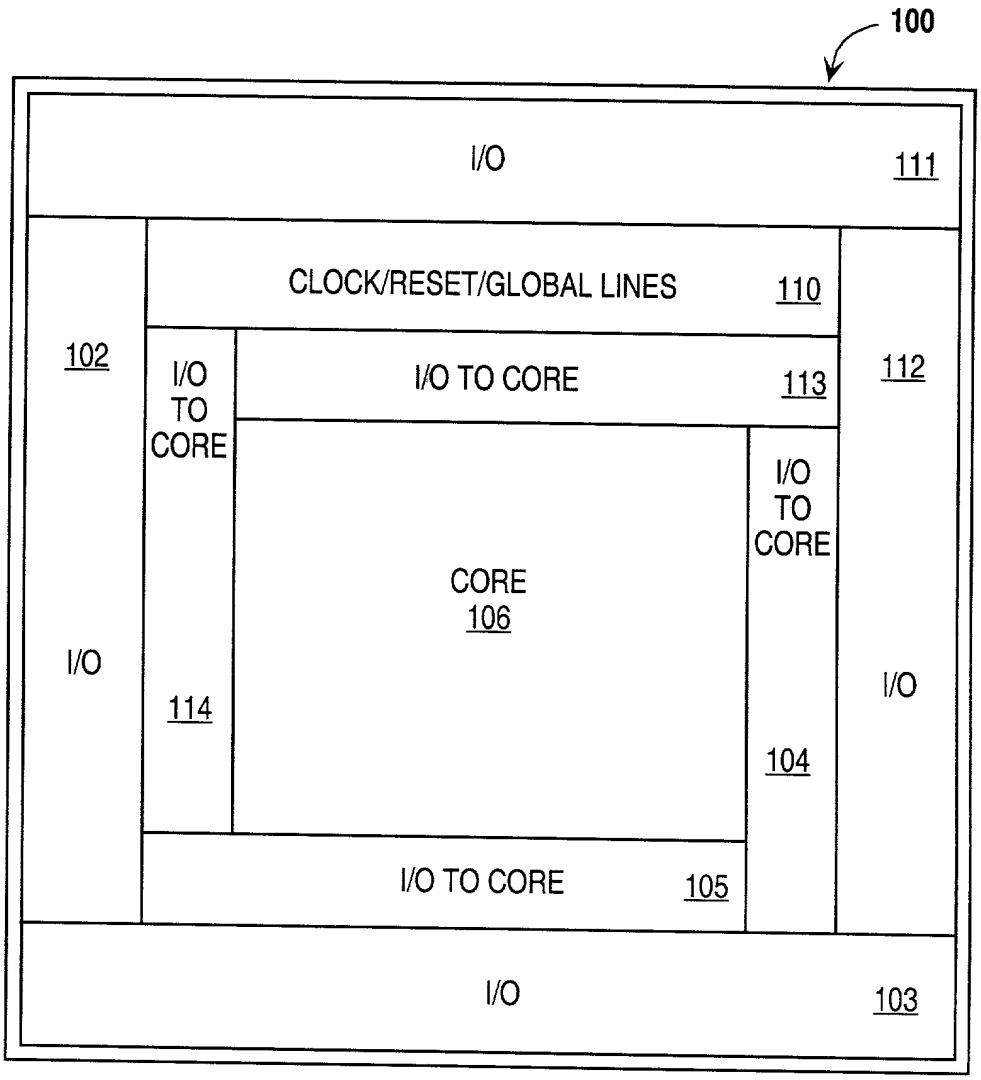

100
I/O
111
CLOCK/RESET/GLOBAL LINES
110
102
I/O TO CORE
113
112
I/O TO CORE
I/O TO CORE
CORE
106
I/O
114
I/O
104
I/O TO CORE
105
I/O
103

FIG. 1

20230 th2t200t

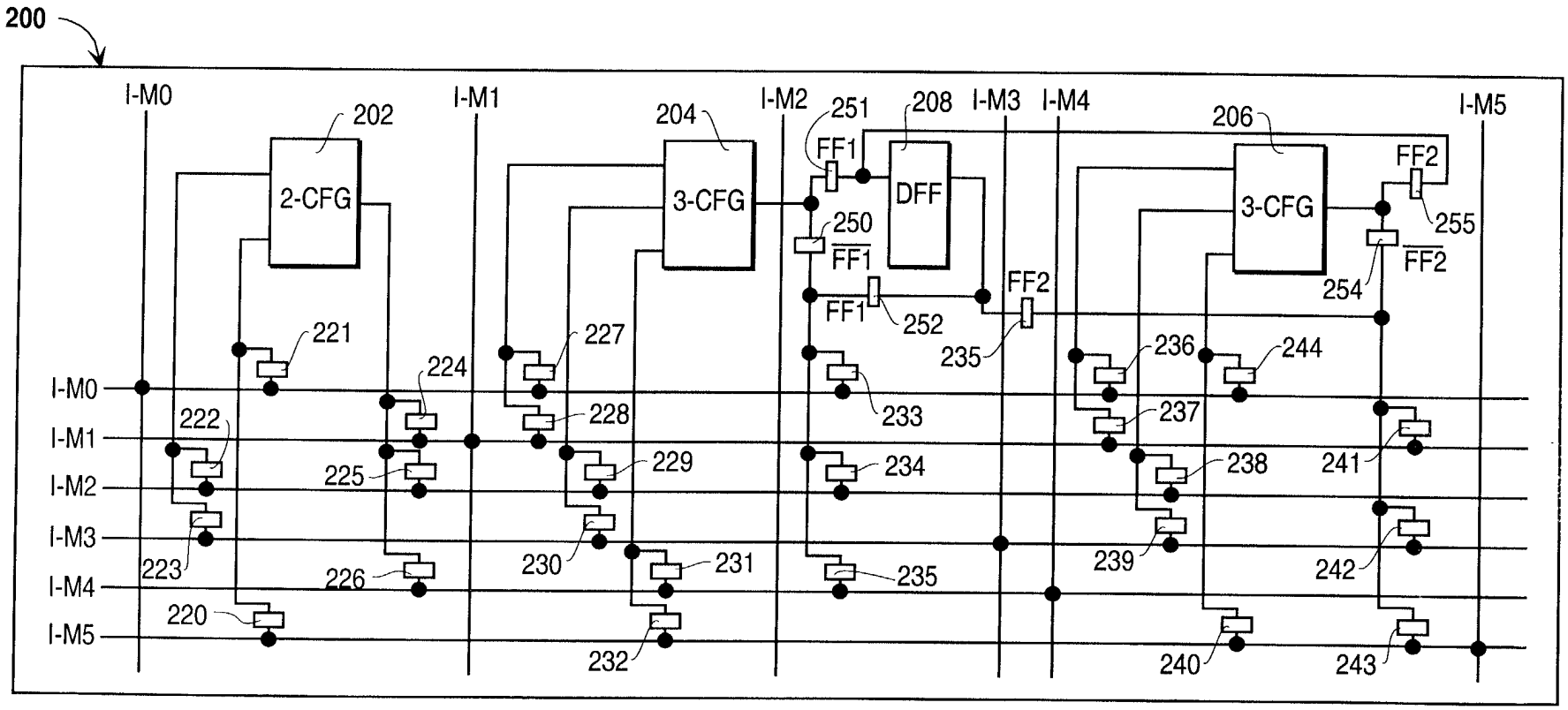


FIG. 2A

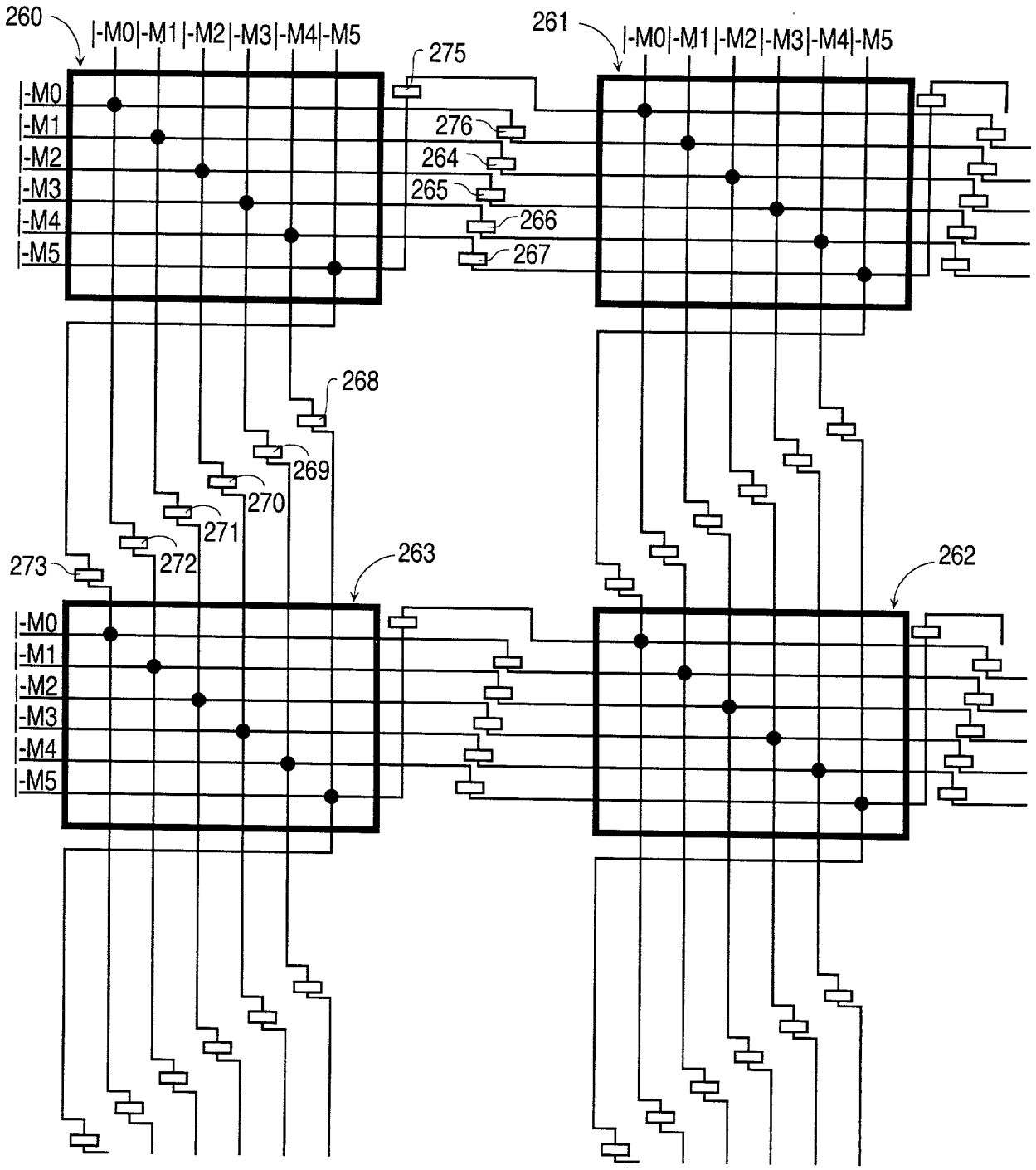

260
|-M0|-M1|-M2|-M3|-M4|-M5
|-M0
|-M1
|-M2
|-M3
|-M4
|-M5
275
261
|-M0|-M1|-M2|-M3|-M4|-M5
276
264
265
266
267
268
269
270
271
272
273
263
262
|-M0
|-M1
|-M2
|-M3
|-M4
|-M5

FIG. 2B

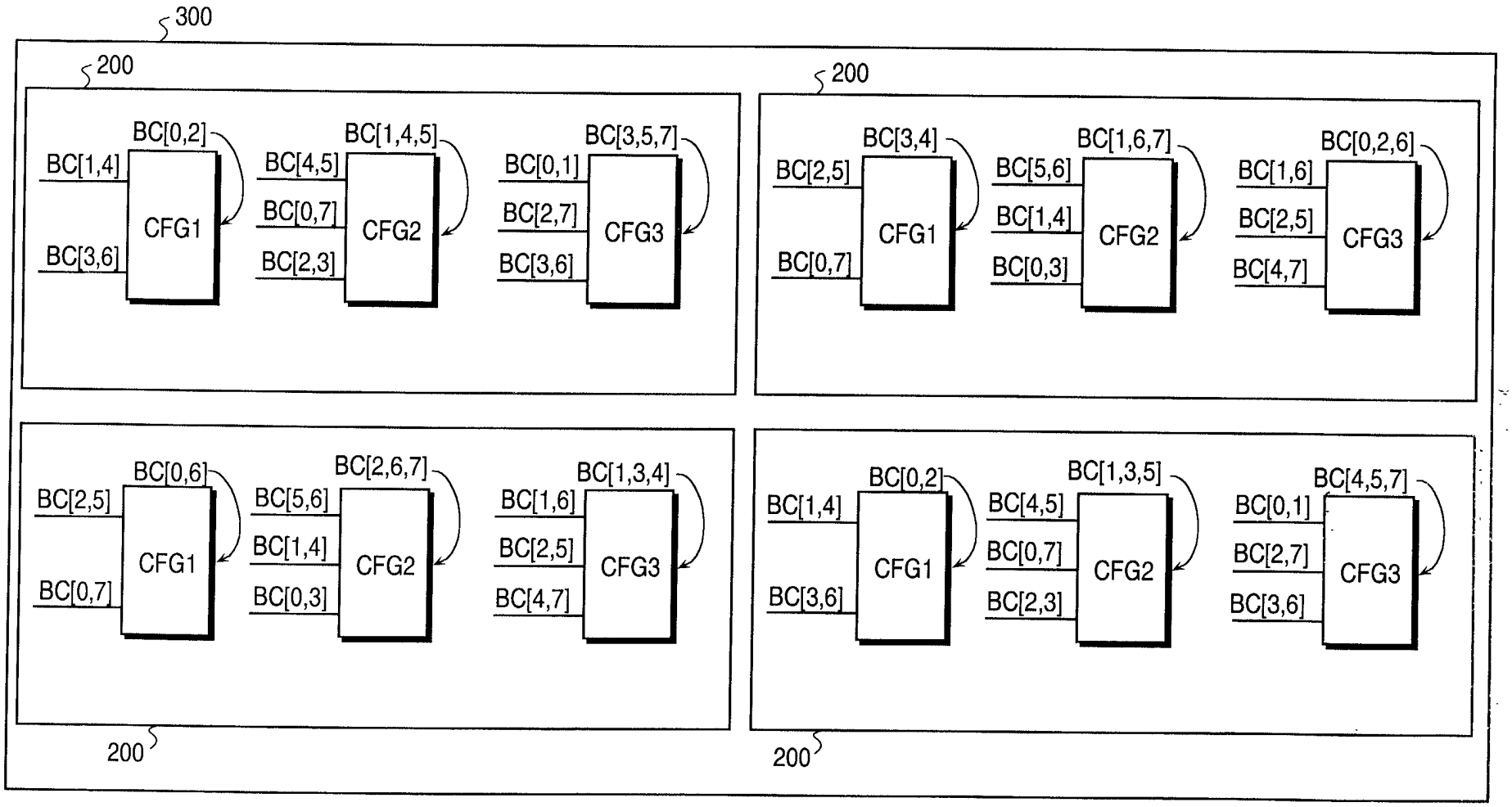

300
200
BC[0,2]
BC[1,4]
BC[3,6]
CFG1
BC[1,4,5]
BC[4,5]
BC[0,7]
BC[2,3]
CFG2
BC[3,5,7]
BC[0,1]
BC[2,7]
BC[3,6]
CFG3
200
BC[3,4]
BC[2,5]
BC[0,7]
CFG1
BC[1,6,7]
BC[5,6]
BC[1,4]
BC[0,3]
CFG2
BC[0,2,6]
BC[1,6]
BC[2,5]
BC[4,7]
CFG3
BC[0,6]
BC[2,5]
BC[0,7]
CFG1
BC[2,6,7]
BC[5,6]
BC[1,4]
BC[0,3]
CFG2
BC[1,3,4]
BC[1,6]
BC[2,5]
BC[4,7]
CFG3
200
BC[0,2]
BC[1,4]
BC[3,6]
CFG1
BC[1,3,5]
BC[4,5]
BC[0,7]
BC[2,3]
CFG2
BC[4,5,7]
BC[0,1]
BC[2,7]
BC[3,6]
CFG3
200

FIG. 3A

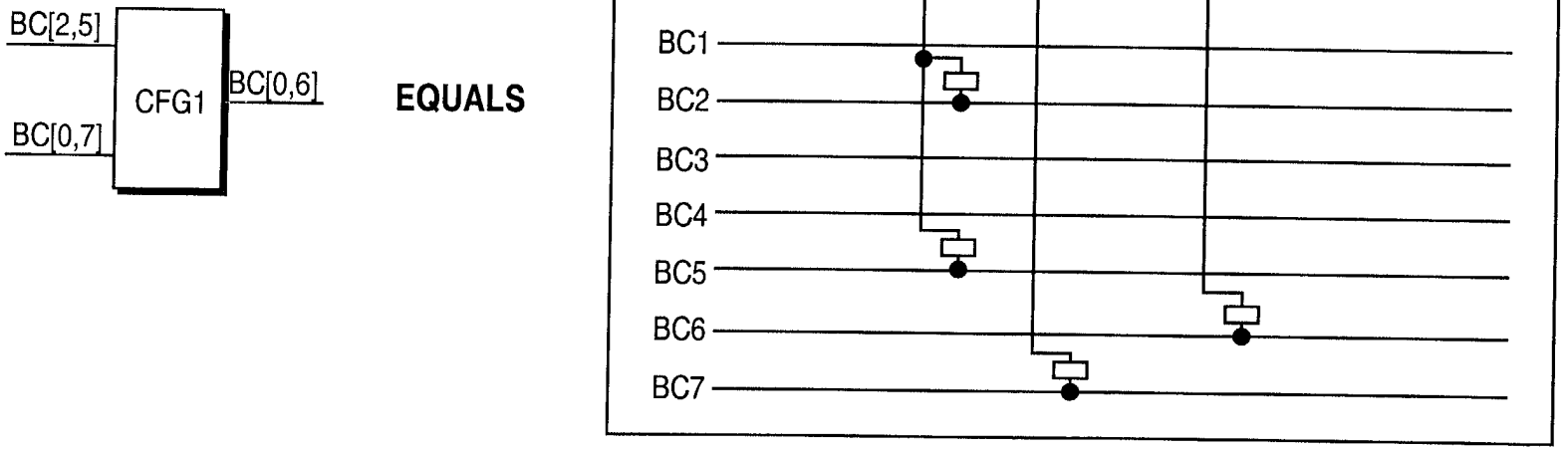

BC[2,5]
BC[0,7]
CFG1
BC[0,6]
EQUALS
BC[2,5]
BC[0,7]
CFG1
BC[0,6]
BC0
BC1
BC2
BC3
BC4
BC5
BC6
BC7

FIG. 3B

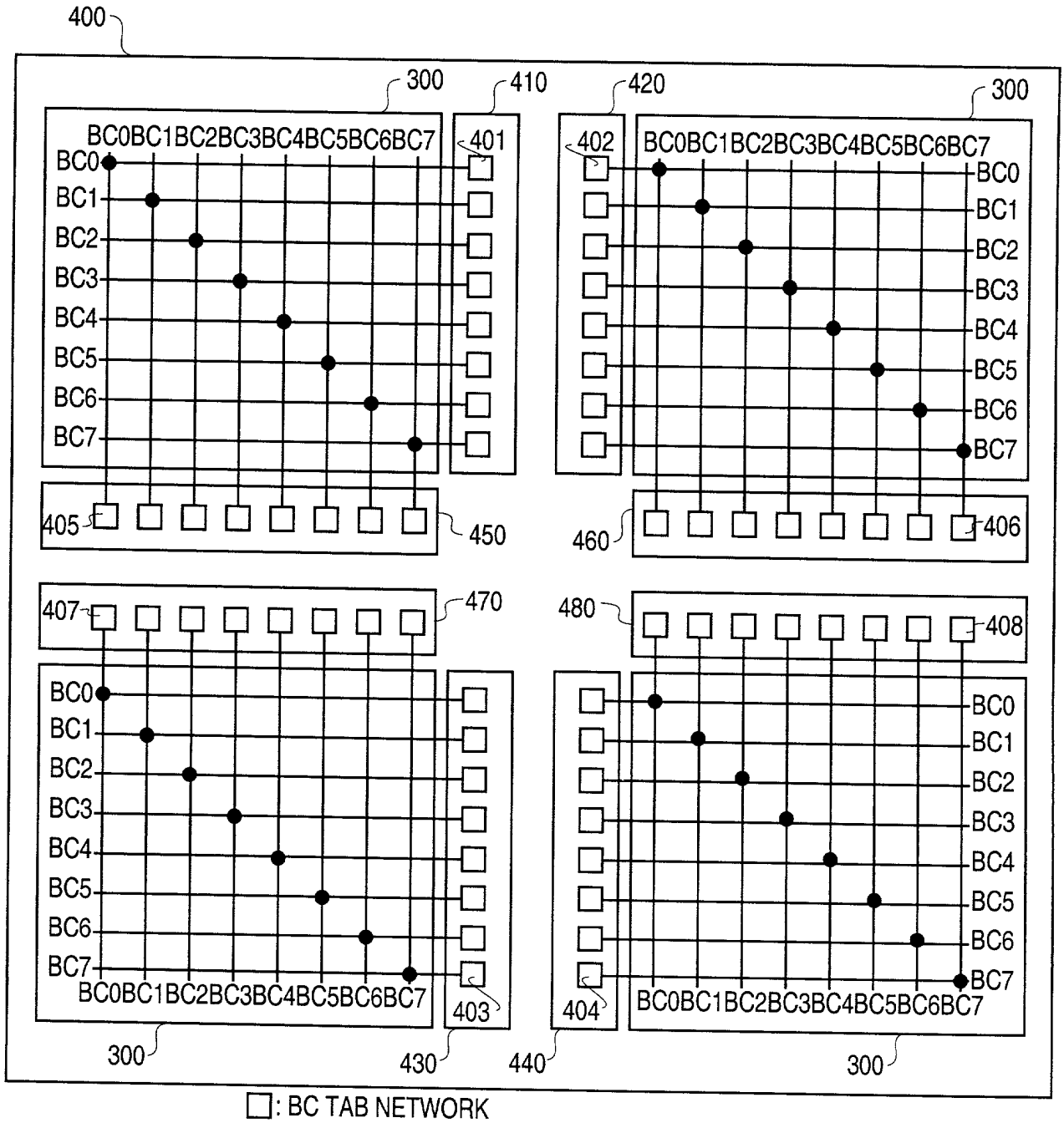

400
300
410
420
300
BC0BC1BC2BC3BC4BC5BC6BC7
401
402
BC0BC1BC2BC3BC4BC5BC6BC7
BC0
BC1
BC2
BC3
BC4
BC5
BC6
BC7
405
450
460
406
407
470
480
408
403
404
430
440
300
300
□: BC TAB NETWORK

FIG. 4A

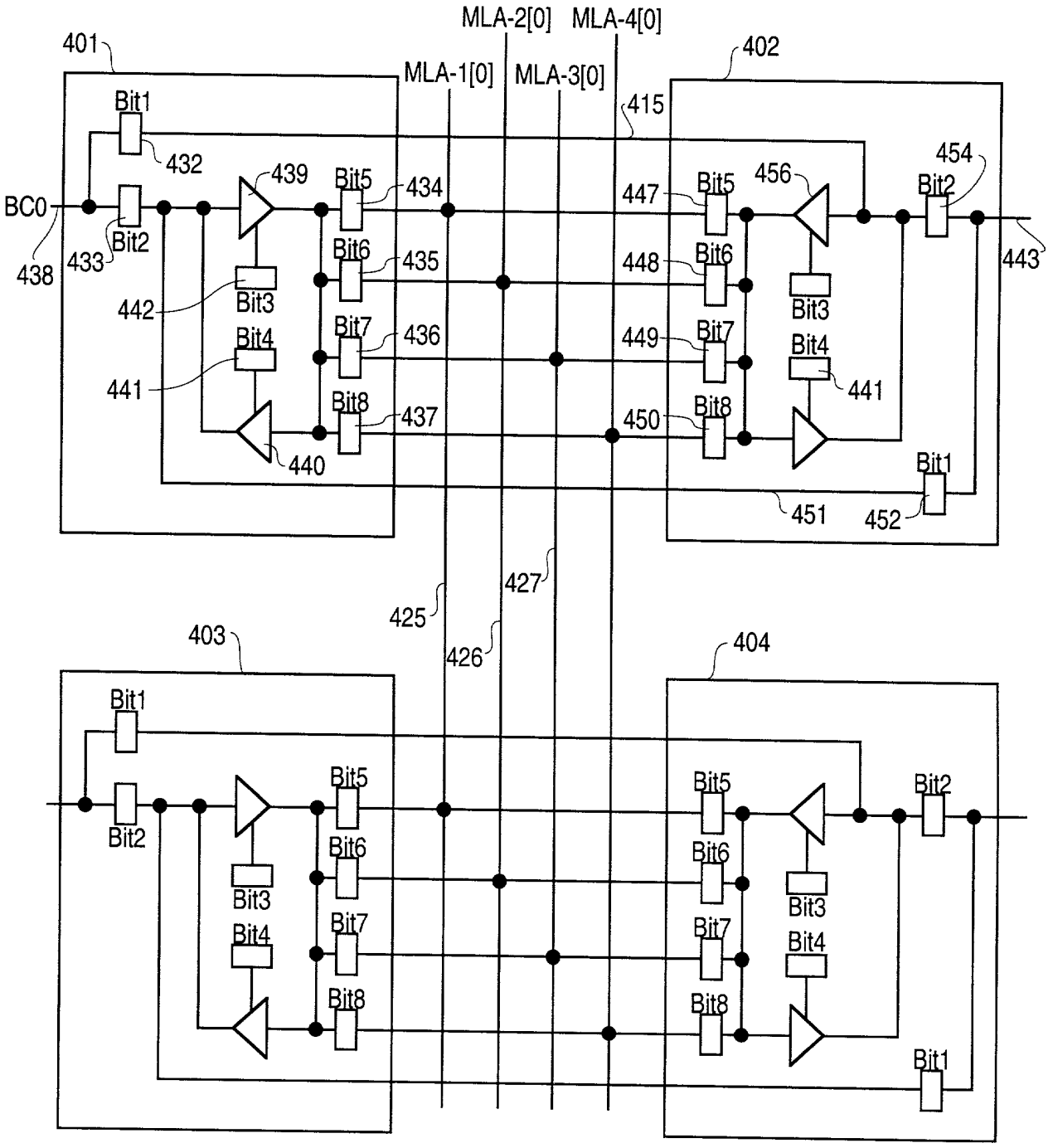

MLA-2[0]
MLA-4[0]
MLA-1[0]
MLA-3[0]
401
402
403
404
415
425
426
427
Bit1
Bit2
Bit3
Bit4
Bit5
Bit6
Bit7
Bit8
BC0
432
433
434
435
436
437
438
439
440
441
442
443
447
448
449
450
451
452
454
456

FIG. 4B

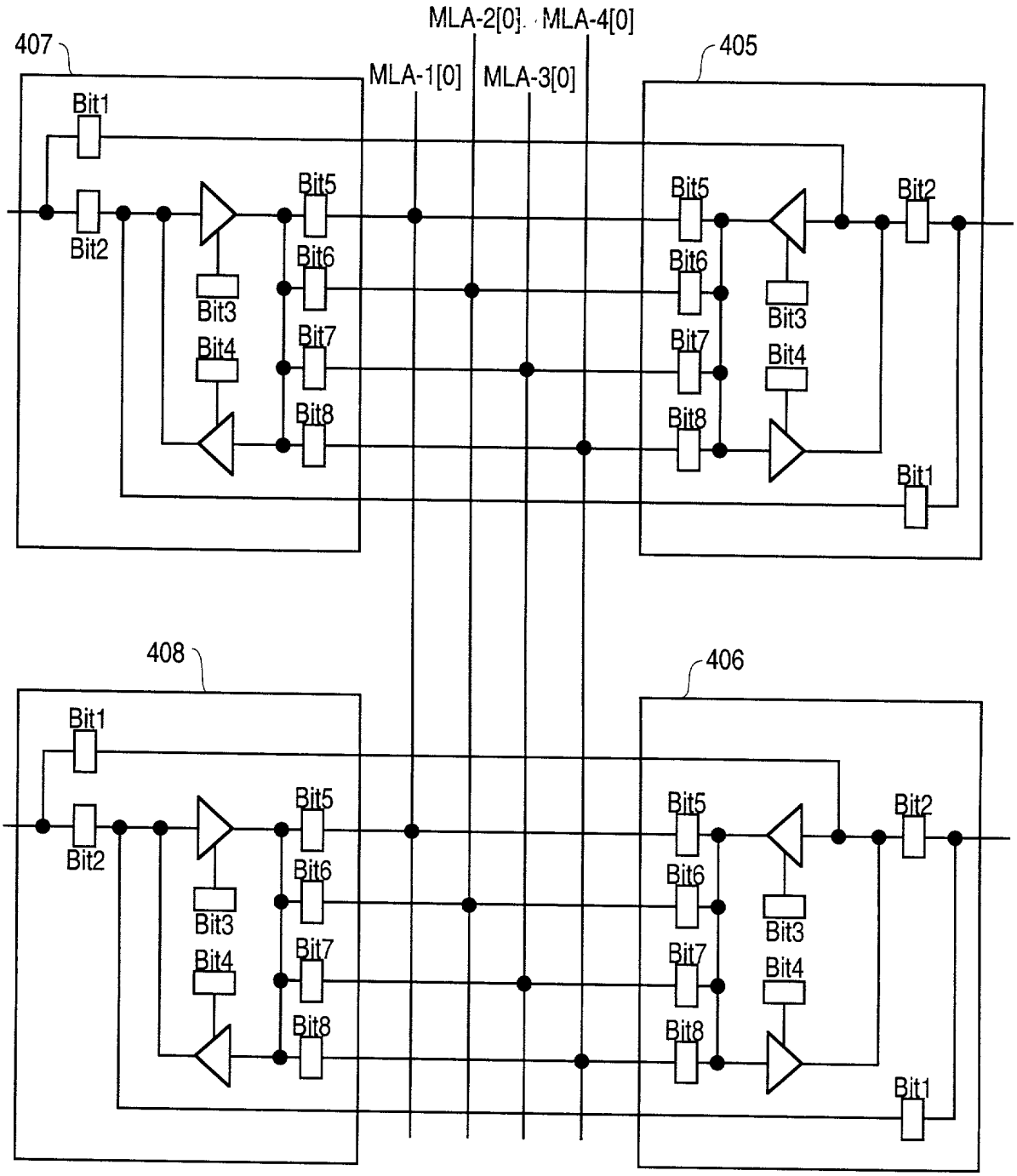

MLA-2[0]
MLA-4[0]
MLA-1[0]
MLA-3[0]
407
405
408
406
Bit1
Bit2
Bit3
Bit4
Bit5
Bit6
Bit7
Bit8

FIG. 4C

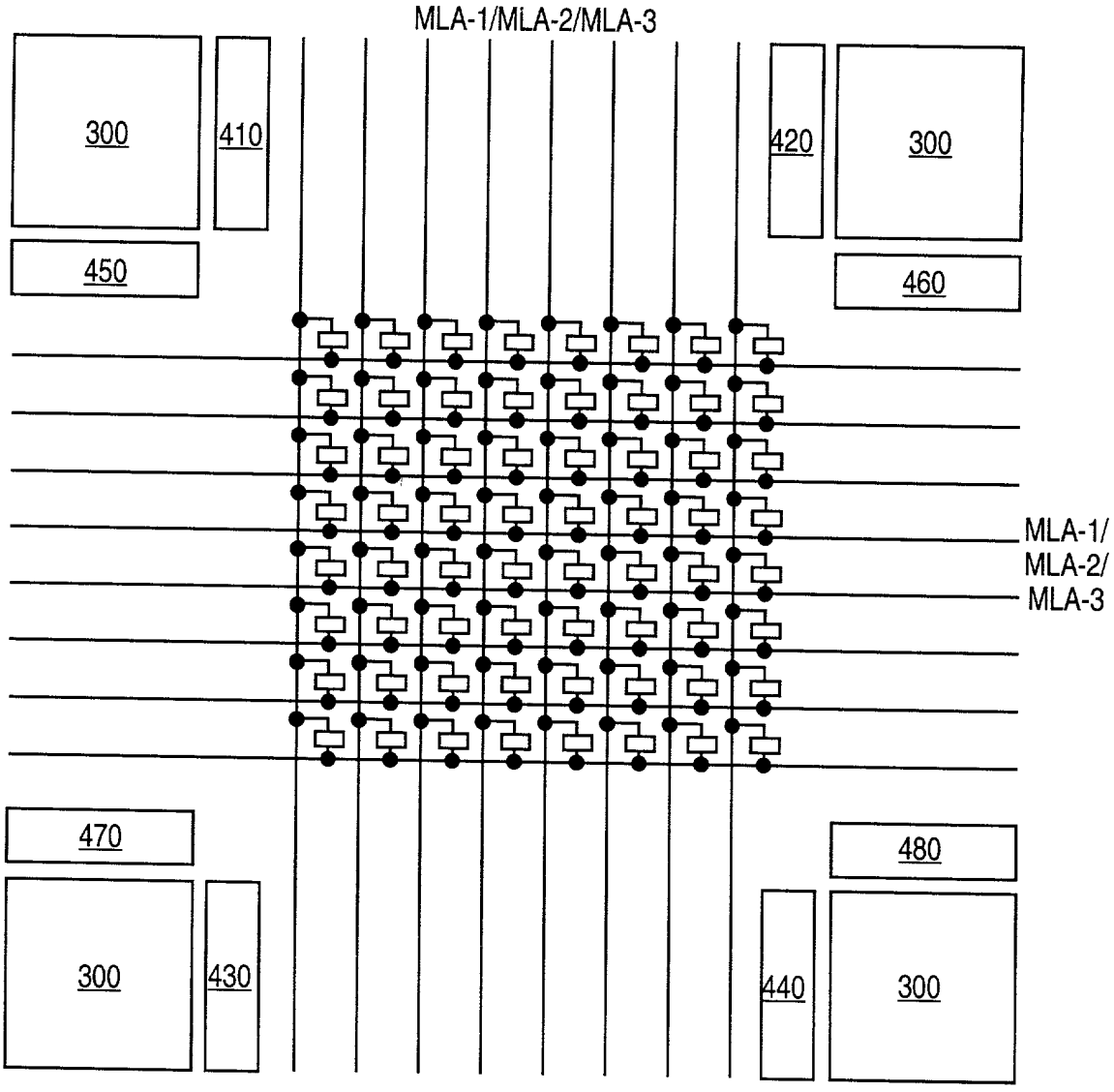

MLA-1/MLA-2/MLA-3
300
410
420
300
450
460
MLA-1/
MLA-2/
MLA-3
470
480
300
430
440
300

FIG. 5

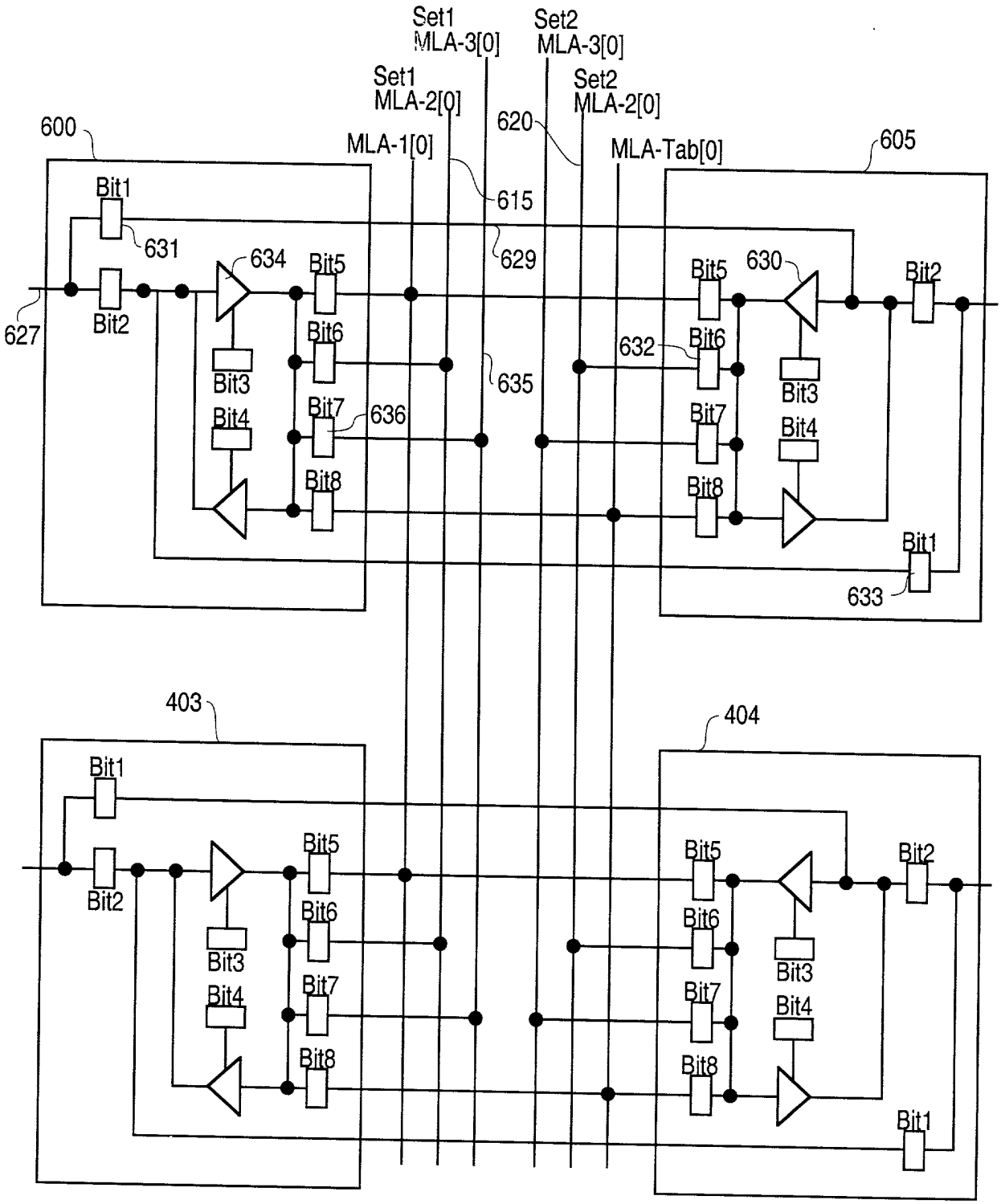

Set1
MLA-3[0]
Set2
MLA-3[0]
Set1
MLA-2[0]
Set2
MLA-2[0]
600
620
MLA-1[0]
MLA-Tab[0]
605
615
Bit1
631
629
634
Bit5
630
Bit2
627
Bit2
Bit6
632
Bit6
Bit3
635
Bit3
Bit7
636
Bit4
Bit7
Bit4
Bit8
Bit8
Bit1
633
403
404
Bit1
Bit5
Bit5
Bit2
Bit2
Bit6
Bit6
Bit3
Bit3
Bit7
Bit4
Bit7
Bit4
Bit8
Bit8
Bit1

FIG. 6A

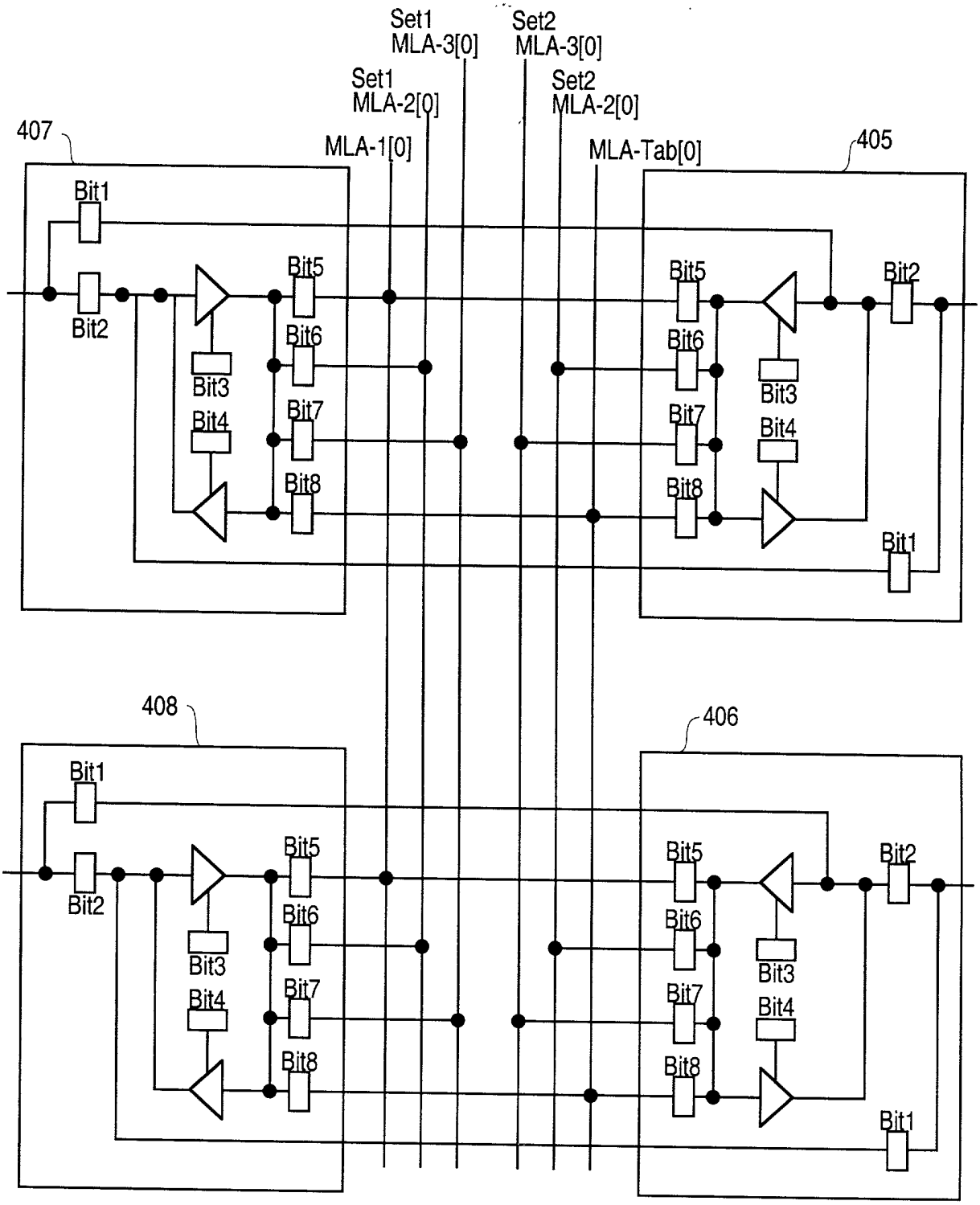

Set1
MLA-3[0]
Set2
MLA-3[0]
Set1
MLA-2[0]
Set2
MLA-2[0]
407
MLA-1[0]
MLA-Tab[0]
405
Bit1
Bit2
Bit5
Bit6
Bit3
Bit4
Bit7
Bit8
Bit5
Bit6
Bit3
Bit7
Bit4
Bit8
Bit2
Bit1
408
406
Bit1
Bit2
Bit5
Bit6
Bit3
Bit4
Bit7
Bit8
Bit5
Bit6
Bit3
Bit7
Bit4
Bit8
Bit2
Bit1

FIG. 6B

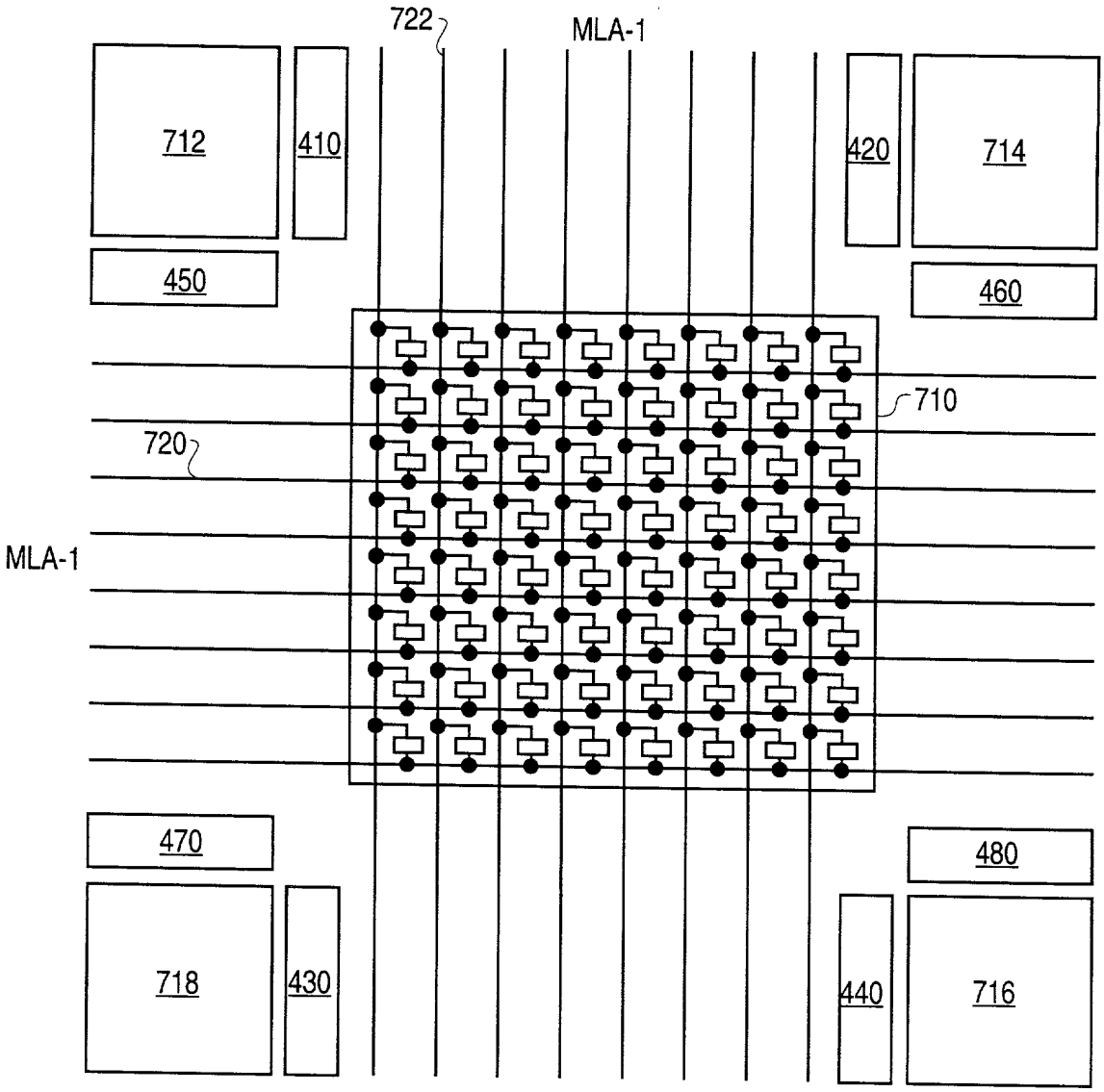

722
MLA-1
712
410
420
714
450
460
710
720
MLA-1
470
480
718
430
440
716

FIG. 7A

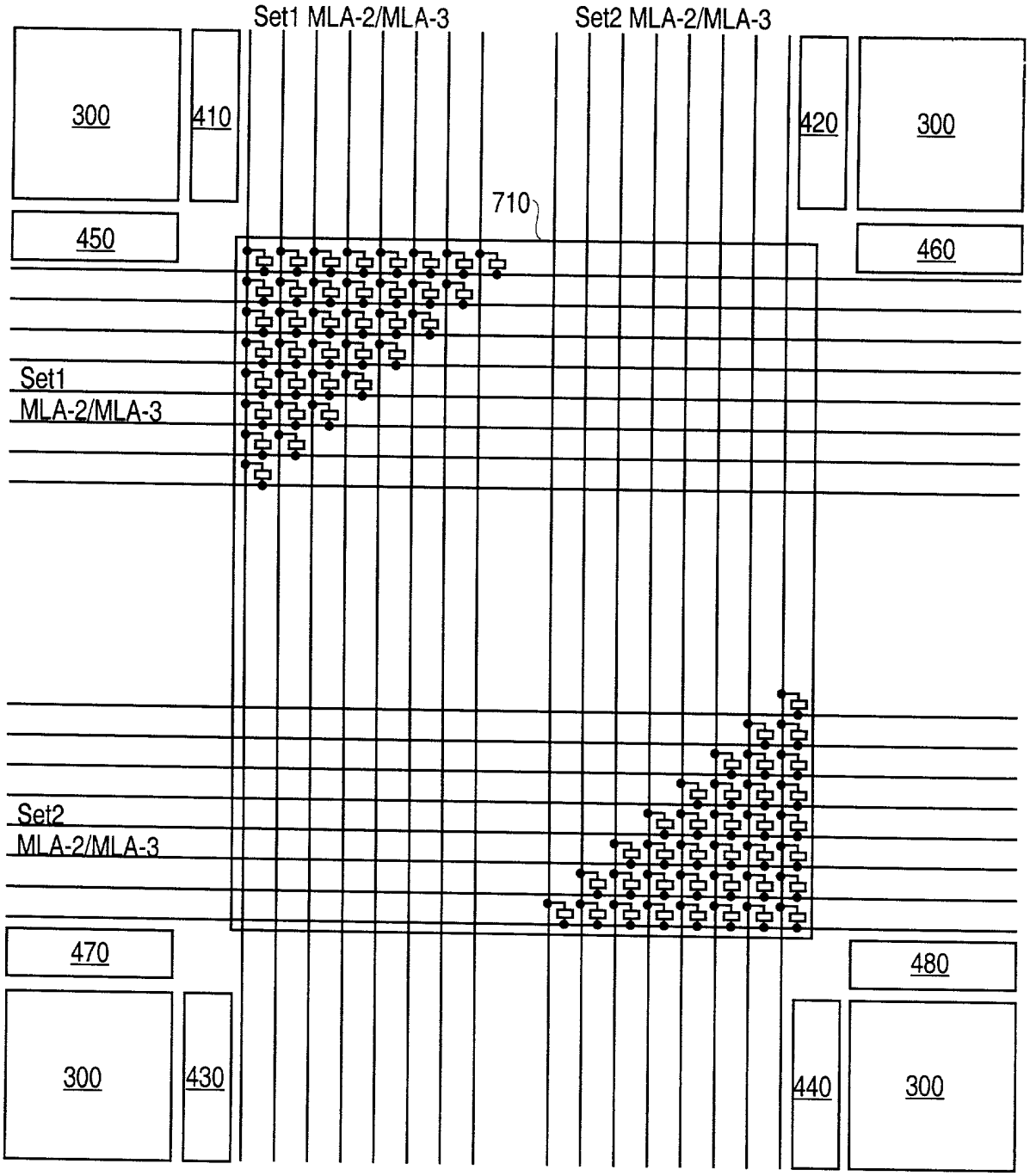

Set1 MLA-2/MLA-3
Set2 MLA-2/MLA-3
300
410
420
300
710
450
460
Set1
MLA-2/MLA-3
Set2
MLA-2/MLA-3
470
480
300
430
440
300

FIG. 7B

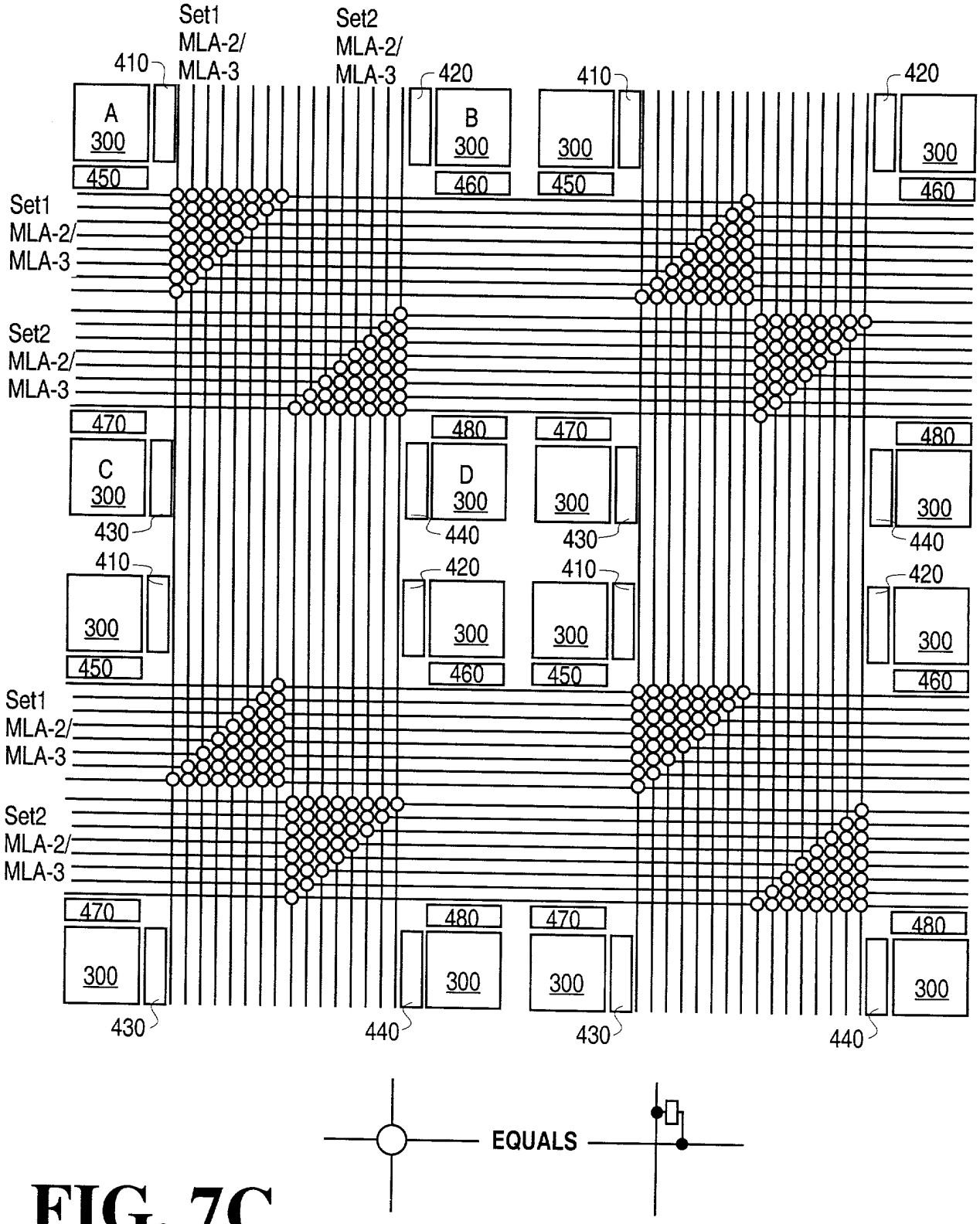

Set1
MLA-2/
MLA-3
Set2
MLA-2/
MLA-3
410
420
A
300
B
300
300
300
450
460
450
460
Set1
MLA-2/
MLA-3
Set2
MLA-2/
MLA-3
470
480
470
480
C
300
D
300
300
300
430
440
430
440
410
420
410
420
300
300
300
300
450
460
450
460
Set1
MLA-2/
MLA-3
Set2
MLA-2/
MLA-3
470
480
470
480
300
300
300
300
430
440
430
440
EQUALS

FIG. 7C

2021-10-14

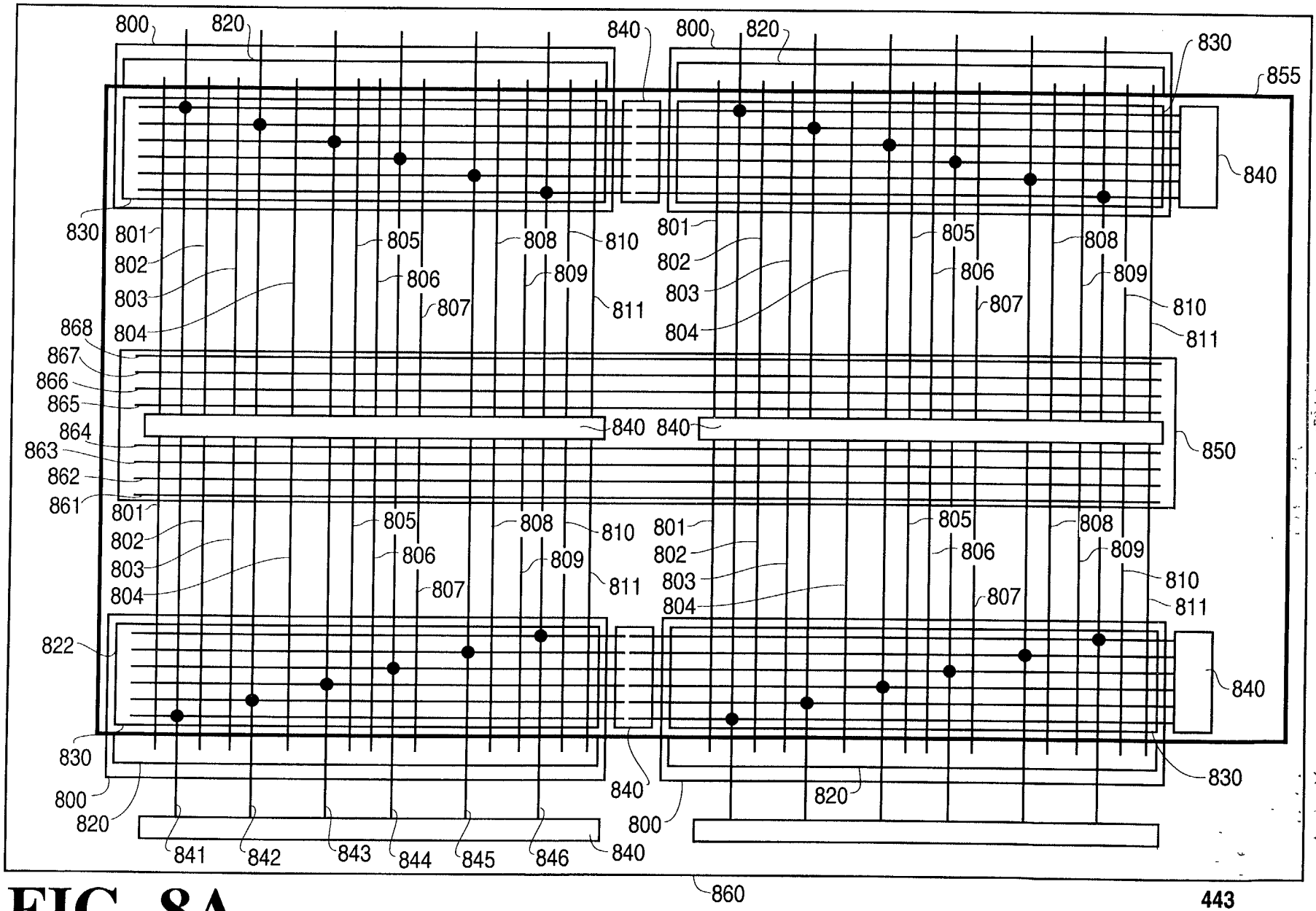


FIG. 8A

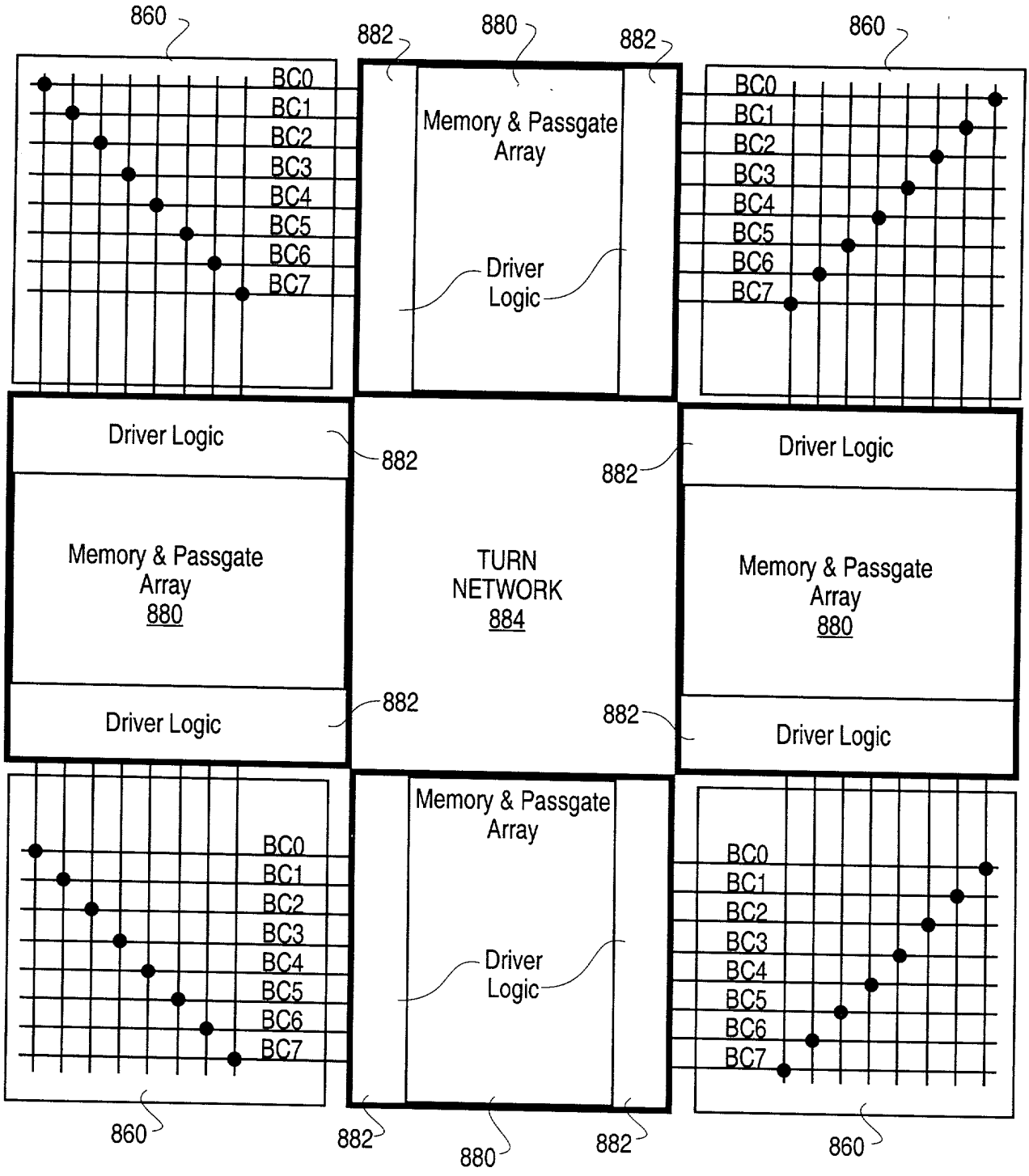
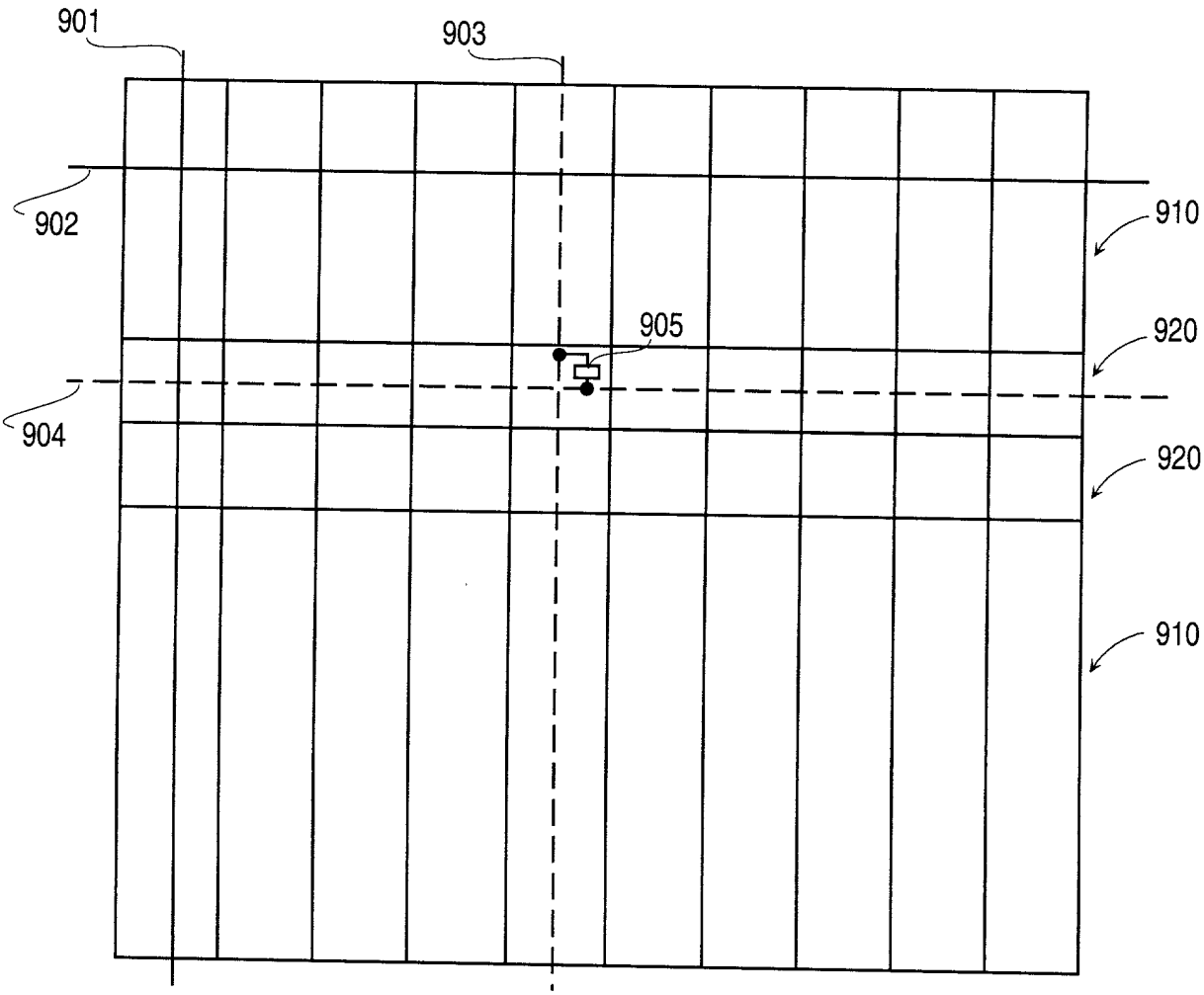

860
882
880
882
860
BC0
BC1
BC2
BC3
BC4
BC5
BC6
BC7
Memory & Passgate Array
Driver Logic
Driver Logic
882
882
Driver Logic
Memory & Passgate Array
880
TURN NETWORK
884
882
882
Driver Logic
Driver Logic
Memory & Passgate Array
880
BC0
BC1
BC2
BC3
BC4
BC5
BC6
BC7
Driver Logic
860
882
880
882
860

FIG. 8B



910 : MEMORY BITS
920 : PASSGATES
901, 902 : ADDRESSING LINES x - y
903, 904 : ROUTING LINES
905 : PROGRAM CONTROLLED PASSGATE BETWEEN 903 AND 904

FIG. 9 EXAMPLE OF CONTIGUOUS MEMORY AND PASSGATE ARRAY LAYOUT ORGANIZATION